

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the layer.

57. (Amended) A memory device, comprising:
  - a memory array;
  - a control circuit operatively coupled to the memory array; and
  - an I/O circuit operatively coupled to the memory array;
  - wherein at least one of the memory array, control circuit and I/O circuit comprises a contact having a titanium alloy layer formed overlying walls of a contact hole and a titanium silicide layer formed overlying an exposed silicon base layer of the contact hole, the titanium silicide layer being directly coupled to the titanium alloy layer, and having a composition that is different from the titanium alloy layer.
60. (Amended) A memory device, comprising:
  - a semiconductor substrate;
  - a memory array coupled to the semiconductor substrate;
  - a control circuit, operatively coupled to the memory array;
  - an I/O circuit, operatively coupled to the memory array;
  - an electronic device coupled to the semiconductor substrate, the electronic device having an active region;
  - an insulating layer over the active region;
  - an alloy layer of a titanium alloy within a contact opening in the insulating layer, the contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and
  - a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.

64. (Amended) A memory device, comprising:
- a semiconductor substrate;
  - a memory array coupled to the semiconductor substrate;
  - a control circuit, operatively coupled to the memory array;
  - an I/O circuit, operatively coupled to the memory array;
  - a transistor formed on the semiconductor substrate, the transistor having a source/drain region;
  - an insulating layer over the source/drain region;
  - an alloy layer of a titanium alloy within a contact opening in the insulating layer, the contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and
  - a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.
68. (Amended) A memory device, comprising:
- a semiconductor substrate;
  - a memory array coupled to the semiconductor substrate;
  - a control circuit, operatively coupled to the memory array;
  - an I/O circuit, operatively coupled to the memory array;
  - an electronic device formed on the semiconductor substrate, the electronic device having an active region;
  - a [borophosphous silicate] borophosphosilicate glass (BPSG) layer over the active region;
  - an alloy layer of a titanium alloy within a contact opening in the [borophosphous silicate] borophosphosilicate glass (BPSG) layer, the contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony;

and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.

72. (Amended) A memory device, comprising:
  - a semiconductor substrate;
  - a memory array coupled to the semiconductor substrate;
  - a control circuit, operatively coupled to the memory array;
  - an I/O circuit, operatively coupled to the memory array;
  - an electronic device coupled to the semiconductor substrate, the electronic device having an active region;
  - an insulating layer over the active region;
  - an alloy layer of a titanium alloy within a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and
  - a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.
76. (Amended) The memory device of claim 72, wherein the insulator layer includes [borophosphorous silicate] borophosphosilicate glass (BPSG).
77. (Amended) A memory device, comprising:
  - a semiconductor substrate;
  - a memory array coupled to the semiconductor substrate;
  - a control circuit, operatively coupled to the memory array;
  - an I/O circuit, operatively coupled to the memory array;
  - a transistor coupled to the semiconductor substrate, the transistor having a source/drain

region;

an insulating layer over the source/drain region;  
an alloy layer of a titanium alloy within a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.

80. (Amended) The memory device of claim 77, wherein the insulator layer includes [borophosphous silicate] borophosphosilicate glass (BPSG).

81. (Amended) A memory device, comprising:

a semiconductor substrate;  
a memory array coupled to the semiconductor substrate;  
a control circuit, operatively coupled to the memory array;  
an I/O circuit, operatively coupled to the memory array;  
a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;

a [borophosphous silicate] borophosphosilicate glass (BPSG) layer over the source/drain region;

an alloy layer of a titanium alloy within a high aspect ratio contact opening in the [borophosphous silicate] borophosphosilicate glass (BPSG) layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

**Clean Version of Pending Claims**

**CHEMICAL VAPOR DEPOSITION OF TITANIUM**

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*Claims 46-47 and 57-82, as of August 30, 2002 (date response to first office action filed).*

46. (Amended) A memory, comprising:  
a memory array;  
a control circuit, operatively coupled to the memory array;  
an I/O circuit, operatively coupled to the memory array; and  
wherein the memory array, control circuit and I/O circuit each comprise:  
a layer of a titanium alloy, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and  
a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the layer.
47. The memory of claim 46, wherein the titanium alloy comprises titanium and zinc.
57. (Amended) A memory device, comprising:  
a memory array;  
a control circuit operatively coupled to the memory array; and  
an I/O circuit operatively coupled to the memory array;  
wherein at least one of the memory array, control circuit and I/O circuit comprises a contact having a titanium alloy layer formed overlying walls of a contact hole and a titanium silicide layer formed overlying an exposed silicon base layer of the contact hole, the titanium silicide layer being directly coupled to the titanium alloy layer, and having a composition that is different from the titanium alloy layer.

58. A memory device, comprising:
- a memory array;
- a control circuit operatively coupled to the memory array; and
- an I/O circuit operatively coupled to the memory array;
- wherein at least one of the memory array, control circuit and I/O circuit comprises a via having a titanium alloy layer formed overlying walls and an exposed base layer of a contact hole and a fill coupled to the titanium alloy layer, wherein the fill comprises a metal selected from the group consisting of tungsten and aluminum.
59. A memory device, comprising:
- a memory array;
- a control circuit operatively coupled to the memory array; and
- an I/O circuit operatively coupled to the memory array;
- wherein at least one of the memory array, control circuit and I/O circuit comprises a titanium layer, wherein the titanium layer is produced using a method, the method comprising:
- forming a seed layer supported by a substrate by combining a first precursor with a first reducing agent; and
- forming the titanium layer supported by the substrate by combining a titanium-containing precursor with the seed layer.
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60. (Amended) A memory device, comprising:
- a semiconductor substrate;
- a memory array coupled to the semiconductor substrate;
- a control circuit, operatively coupled to the memory array;
- an I/O circuit, operatively coupled to the memory array;

33

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy within a contact opening in the insulating layer, the

contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.

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61. The memory device of claim 60, wherein the titanium alloy includes titanium and zinc.

62. (The memory device of claim 60, wherein the insulator layer includes silicon dioxide ( $\text{SiO}_2$ ).

63. The memory device of claim 60, wherein the electronic device includes a transistor.

64. (Amended) A memory device, comprising:

    a semiconductor substrate;

    a memory array coupled to the semiconductor substrate;

    a control circuit, operatively coupled to the memory array;

    an I/O circuit, operatively coupled to the memory array;

    a transistor formed on the semiconductor substrate, the transistor having a source/drain region;

    an insulating layer over the source/drain region;

    an alloy layer of a titanium alloy within a contact opening in the insulating layer, the

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contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and  
a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.

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65. The memory device of claim 64, wherein the titanium alloy includes titanium and zinc.

66. The memory device of claim 64, wherein the insulator layer includes silicon dioxide ( $\text{SiO}_2$ ).

67. The memory device of claim 64, wherein the contact opening includes a high aspect ratio contact opening.

*B5*

68. (Amended) A memory device, comprising:  
a semiconductor substrate;  
a memory array coupled to the semiconductor substrate;  
a control circuit, operatively coupled to the memory array;  
an I/O circuit, operatively coupled to the memory array;  
an electronic device formed on the semiconductor substrate, the electronic device having an active region;  
a borophosphosilicate glass (BPSG) layer over the active region;  
an alloy layer of a titanium alloy within a contact opening in the borophosphosilicate glass (BPSG) layer, the contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium,

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tin, silicon, germanium, lead, arsenic and antimony; and  
a titanium silicide contact having a composition that is different from the layer of  
titanium alloy, the contact being directly coupled to the alloy layer.

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69. The memory device of claim 68, wherein the titanium alloy includes titanium and zinc.
70. The memory device of claim 68, wherein the electronic device includes a transistor.
71. The memory device of claim 68, wherein the contact opening includes a high aspect ratio contact opening.
  
72. (Amended) A memory device, comprising:  
*B6*  
a semiconductor substrate;  
a memory array coupled to the semiconductor substrate;  
a control circuit, operatively coupled to the memory array;  
an I/O circuit, operatively coupled to the memory array;  
an electronic device coupled to the semiconductor substrate, the electronic device having  
an active region;  
an insulating layer over the active region;  
an alloy layer of a titanium alloy within a high aspect ratio contact opening in the  
insulating layer, the high aspect ratio contact opening being at least partially over  
the active region, wherein the titanium alloy comprises titanium and an element  
selected from the group consisting of zinc, cadmium, mercury, aluminum,  
gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and  
a titanium silicide contact having a composition that is different from the layer of  
titanium alloy, the contact being directly coupled to the alloy layer.

73. The memory device of claim 72, wherein the titanium alloy includes titanium and zinc.

74. The memory device of claim 72, wherein the electronic device includes a transistor.

75. The memory device of claim 72, wherein the insulator layer includes silicon dioxide ( $\text{SiO}_2$ ).

*B7*  
76. (Amended) The memory device of claim 72, wherein the insulator layer includes borophosphosilicate glass (BPSG).

77. (Amended) A memory device, comprising:  
a semiconductor substrate;  
a memory array coupled to the semiconductor substrate;  
a control circuit, operatively coupled to the memory array;  
an I/O circuit, operatively coupled to the memory array;  
a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;

an insulating layer over the source/drain region;  
an alloy layer of a titanium alloy within a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and  
a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.

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78. The memory device of claim 77, wherein the titanium alloy includes titanium and zinc.

79. The memory device of claim 77, wherein the insulator layer includes silicon dioxide ( $\text{SiO}_2$ ).

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80. (Amended) The memory device of claim 77, wherein the insulator layer includes borophosphosilicate glass (BPSG).  
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81. (Amended) A memory device, comprising:  
a semiconductor substrate;  
a memory array coupled to the semiconductor substrate;  
a control circuit, operatively coupled to the memory array;  
an I/O circuit, operatively coupled to the memory array;  
a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;  
a borophosphosilicate glass (BPSG) layer over the source/drain region;  
an alloy layer of a titanium alloy within a high aspect ratio contact opening in the borophosphosilicate glass (BPSG) layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and  
a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.

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82. The memory device of claim 81, wherein the titanium alloy includes titanium and zinc.